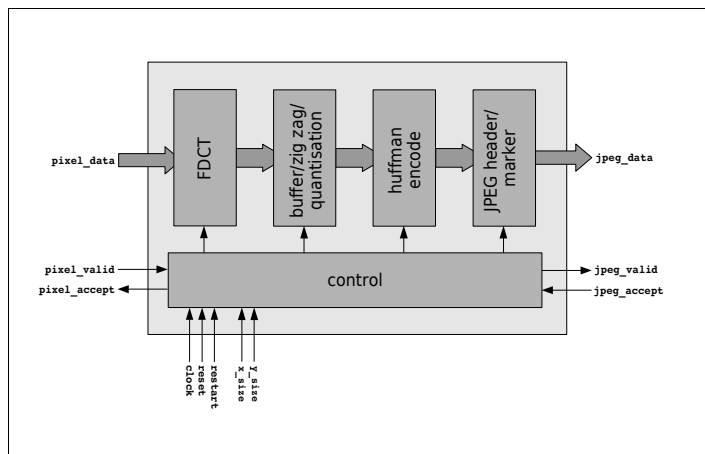




Greyscale JPEG Encoder Datasheet



Features

- Supports baseline JPEG encode as per ISO/IEC 10918-1
- Encodes one pixel every clock cycle
- Configured by hard coded defaults or microprocessor interface
- Supports image sizes up to 64k x 64k
- 8 bits per pixel
- Simple valid-accept interfaces for easy integration
- Available optimised for both ASIC and FPGA

Description

The Art of Silicon Greyscale JPEG Encoder supports high speed baseline progressive JPEG encode. It is available with predefined tables (as suggested by ISO/IEC 10918-1) or may alternatively be configured via a microprocessor interface.

All internal state is clocked from a single clock input. A synchronous reset is provided. Clock and reset senses are configurable.

This block is available as an optimized FPGA bitstream or verilog source code for ASIC designs. A full testbench and test suite is included with the design.

Implementation Results for hard coded table variant

Family	Frequency (MHz)	Slices	Block Rams	18x18 Muls
Lattice ECP2	>90	2695	5	6
Lattice ECP2M	>90	2683	5	6
Lattice SC	>125	3514	5	-
Lattice XP	>50	3316	5	-
Lattice XP2	>65	2659	5	6

Please contact Art of Silicon for more information on the microprocessor interface variant.

Deliverables

- Documentation
- EDIF Netlist or RTL
- Instantiation Template
- Constraints
- Testbench
- Reference C Model

Art of Silicon IP

This is one member of a family of Intellectual Property available from Art of Silicon. Each block is designed with simple interfaces for ease of integration into your designs. We are also happy to customise our IP to your requirements. Telephone and email support is available for all our IP.

Contact Art of Silicon for pricing and ordering information.

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