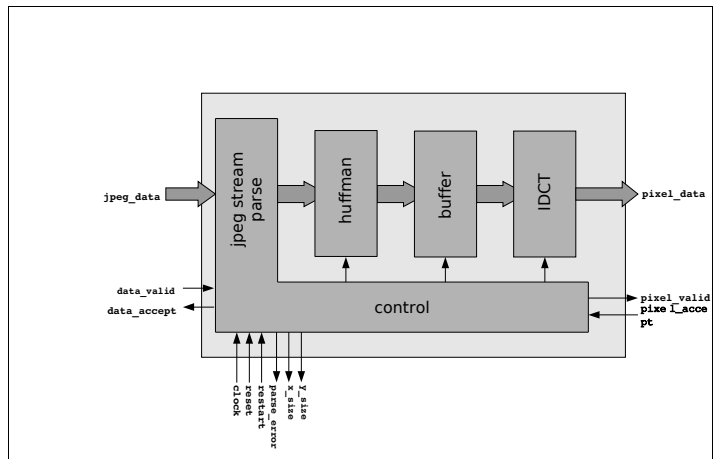




Greyscale JPEG Decoder Datasheet



Features

- Supports baseline JPEG decode as per ISO/IEC 10918-1
- Motion JPEG decoding
- Decodes up to 4 pixels per clock cycle
- Average throughput >1 pixels per cycle
- Self configuring by parsing JPEG header
- Supports image sizes up to 64k x 64k
- 8 bits per pixel
- Simple valid-accept 32-bit interfaces for easy integration
- Available optimised for both ASIC and FPGA

Description

The Art of Silicon Greyscale JPEG decoder supports high speed baseline JPEG decode. It is self configuring by reading header information from an incoming JPEG data stream. Any errors in the JPEG stream are detected and flagged.

All internal state is clocked from a single clock input. A synchronous reset is provided. Clock and reset senses are configurable.

This block is available as an optimized FPGA bitstream or verilog source code for ASIC designs. A full testbench and test suite is included with the design.

Implementation Results

Family	Frequency (MHz)	Slices	Block Rams	18x18 Muls
Lattice ECP2	>100	2831	14	7
Lattice ECP2M	>100	2768	14	7
Lattice SC	>120	3283	14	-
Lattice XP	>55	3345	14	-
Lattice XP2	>75	2849	14	7

Deliverables

- Documentation
- EDIF Netlist or RTL
- Instantiation Template
- Constraints
- Testbench
- Reference C Model

Art of Silicon IP

This is one member of a family of Intellectual Property available from Art of Silicon. Each block is designed with simple interfaces for ease of integration into your designs. We are also happy to customise our IP to your requirements. Telephone and email support is available for all our IP.

Contact Art of Silicon for pricing and ordering information.

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